



## An Efficient Implementation of IS-95A CDMA Transceivers through FPGA

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### Abstract

In this paper, proficient architectures for IS-95A CDMA Transceivers are modeled and optimized for hardware implementation on FPGA. The efficiency of the transceivers is improved by incorporating a novel Interleaver, developed for mobile communication channel. The Interleaver improves the performance of the transceivers at lower SNR levels. The architecture applies a new-fangled scheme for implementing Viterbi decoder and thereby results in reduced computation operations and memory requirements. The model is implemented in Xilinx V100CS144 chip using VHDL. The FPGA hardware uses 88% of a 1200 slice VIRTEX FPGA device and delivers a satisfactory performance with a reduction in memory by 7.6% (for rate 1/2), 40.9% (for rate 1/3) and with maximum net delays much within the allowable limits of maximum data rate of 9.6Kbps.

**Keywords:** IS-95 A CDMA, Interleaver, Viterbi Decoder, Field Programmable Gate array (FPGA), VHDL

### 1. Introduction

Cellular technology has grown tremendously, both in terms of traffic and the services it offers [1-2]. One of the most promising cellular standards is the IS-95A Code Division Multiple Access (CDMA) system. The advantages of IS-95A CDMA standard over other standards are Optimum subscriber Station Power Management, Bandwidth Recycling, Efficient Power Control, Provision of Soft handoffs, Multi Layered Diversity and Compatibility with variable rate vocoders. Service providers are deploying these systems in their markets, where there are mounting demands for higher capacity [3-4]. The forward link frequency is in the range of (869-894) MHz and the reverse link frequency is in the range of (824-849) MHz. The forward and reverse architectures are referred from [5-6]. In Mobile Communication transmission from the base station to mobile receiver are on the forward link and the transmission from the mobile user to the base station are on the reverse link.

In the recent years the IS-95A CDMA transceivers, on a FPGA platform has attracted the attention of

academic, research and industry community [7-8]. Most of the reputed literature discusses the design of Traffic channel since the architectures of sync, pilot, and paging channels in the forward link and the access channels in the reverse link are subsets of the traffic channel. A typical Forward Link and Reverse Link Traffic Channel Architectures are shown in figures 1 and 2. The building blocks of a Transceiver consists of Convolutional encoder, Long Code generator, Short Code generator, CRC error detectors, Frame error rate detector, Power control scheme, Walsh Code generator, Data Burst Randomizer, Block interleaver, orthogonal modulator, De-interleaver and Viterbi decoder. In this paper a High performance and low cost IS-95 A Transceiver is realized by designing a novel interleaver and a Viterbi decoder. The complete IS 95A transceiver along with the proposed block interleaver and Viterbi decoder is implemented on a XILINX Virtex FPGA and tested.

The remainder of the paper is organized as follows: Section (2) focuses on Conventional Block Interleaver and proposed interleaver, Section (3) emphasizes on Convolutional decoding, Section (4) concentrate on Viterbi Decoder implementation, Section (5) focuses on Results and Conclusion.

### 2. Conventional Block Interleaver

Interleaving is a process of permuting the data bits according to a pre-defined mapping. It is usually performed at the output of the channel encoder and before the modulation step. The corresponding de-interleaver uses the inverse mapping to restore the original sequence of the data bits obtained from demodulator and passes the output to the channel decoder. The process of interleaving [9] separates consecutive bits wide apart and thereby avoiding burst errors to a superior degree. The effect of interleaving is equivalent to multiplying the input sequence by a permutation matrix, which corresponds to a linear operation [10]. Block interleavers work on a block of encoded data bits. The bits received from the encoder are stored in the interleaver's memory by filling the columns of an array. After the array is completely filled the bits are read row-by-row and fed to the modulator,



which then transmits them over the channel. Block rectangular interleaving is best expressed in Figure 3. For large block size interleavers, most random interleavers perform well. On the other hand, for some applications it is preferable to have a deterministic interleaver, to reduce the hardware requirements for interleaving and de-interleaving operations. One of the goals of this paper is to propose a deterministic interleaver design to address this problem. In IS-95A CDMA architecture an Intra-frame Rectangular Block interleaving is performed on each frame length [5-6]. It writes in column wise and reads out row wise. It maintains 2 memory pages of size (16 x 24) each. When one is being written on, the other is read out. Each page contains a single instance of data for one 20 ms frame.

Conceptually bits are written in to a two dimensional matrix row wise and read it from column wise. Convolutional encoder of rate 1/2 creates two symbols for each bit data and allows error correction at the receiver. Each symbol is repeated once and a block of 128 of these is interleaved which means to re-order ( Scatter) them with in the block to provide temporal diversity. This is a means of mitigating burst errors to improve error correction when the symbols are decoded at the receiver.

**2.1. Proposed Interleaver:**

For short block length interleavers, selection of the interleaver has a significant effect on the performance of the Convolutional code. The randomness is much improved by following proposed N mod M scheme and thereby the burst errors can be reduced. The mapping equation between the input and output bit positions of the N mod M Interleaver with, x as the output bit position and F(x) as the corresponding input bit position is given by (1)

$$F(x) = (x*N) \text{ mod } M \quad (1)$$

In IS-95A CDMA standard, the number of bits in a page at anytime is a constant and is 384 (16 x 24) and hence M takes on the value of 385 to ensure a one-to-one mapping between the input and the output. The variable x takes on non-repeating values over [1,384]. By substituting various values for N it is found that it is much more efficient to use N=18 interleaving (that is exemplified below) than to use the conventional Rectangular Interleaver. The mapping of the proposed interleaver is given below.

*Output bit position = 10*

*Input bit position = (10\*18) mod 385 = 180*

**3. Convolutional Decoding**

The Viterbi algorithm is commonly used for decoding the convolutional code, a widely used channel decoding techniques [11]. The Viterbi algorithm is to find a maximum-likelihood sequence of state transitions, equivalently a path, in a trellis by assigning a transition metric to possible state transitions. A transition metric is called a branch metric, and the cumulative branch metrics along the path from the initial state to a given state is called the path metric of the state. When two or more paths end at the same state, the path with the smallest (or largest) path metric is selected as the most likely path. The survivor path obtained by back tracing in time

corresponds to the decoded output. The configuration of the convolution codes is disparate in each communication standard which imparts different requirements of the viterbi decoder. Thus a reconfigurable Viterbi decoder with low power consumption and high throughput is a key challenge for future portable devices. Viterbi decoding has the advantage that it has a fixed decoding time but its computational requirements grow exponentially as a function of the constraint length, so it is usually limited in practice to a constraint lengths of K = 9 or less.

The recent related works reveal that the implementation of the Viterbi decoder on FPGA is certainly a contemporary issue. In [12] the authors have implemented a systolic array based Adaptive Viterbi decoder with constraint length 9 and a code rate of 1/2 using XILINX Virtex II Xc 2v1000 FPGAs. In [13] a Reconfigurable Viterbi decoder based on an area efficient Add-compare-select(ACS) Architecture with constraint length varying from 7 to 10 implemented using Xilinx Virtex device is presented. In [14] another Reconfigurable Viterbi fabric with constraint length ranging from 3 to 9 and code rate of 1/2 - 1/3 is implemented using Xilinx Virtex-E FPGA device. Conventional Viterbi decoders, those discussed above suffers from the fact that they require enormous amount of memory. The memory wasted is due to the storing up of error metric at each state and at each level. The wastage can be avoided by the proposed scheme.

**4. A New-Fangled Scheme for Viterbi Decoder Implementation**

The Viterbi decoder that decodes the convolutional encoded data with a rate of k/n ( Number of bits into convolutional encoder (k)/ number of bits in output symbol(n)) , Constraint length K and frame length L bits, consists of the following three functional units as seen in Figure 4.

- Encoder Engine
- Branch metric generator
- Add-Compare-Select (ACS) unit

And three RAM Tables

- Branch and Path Metric Memory
- Present State Memory
- Survivor Memory

The encoder Engine replicates the Convolutional encoder at the receiver and calculates the next state and the output for the various given states and inputs simultaneously. This reduces the memory requirement of the entire trellis structure.

$2 * 2^{(k-1)} * n$  XOR operations are performed with the received n bits and the generated output n bits at each of the  $2^{(k-1)}$  states in the branch metric unit. Parallel architecture is used to enhance the speed of the decoder Branch metric unit is used to calculate branch metrics. The branch metrics are difference values between received code symbol and the corresponding branch words from the encoder trellis. The Path Metric Unit calculates new path metric values and decision values. Because each state can be achieved from two states from



the earlier stage, there are two possible path metrics coming to the current state. The Path Metric Unit adds the branch metric to path metrics and typically selects the smaller one and makes decision. The Path Metric Unit stores the result of the addition as path metric for current state. An Add Compare Select (ACS) unit receives two branch metrics and path metrics. It adds each incoming the corresponding path metric and compares the two results to select a smaller one. The path metric of the state is updated with the selected one. An ACS unit can be time-shared between multiple modules, but it incurs more power dissipation due to the control circuitry. Survivor Path Memory stores the survivor path of each state selected by the ACS module. The number of registers used in this memory is equal to the number of states (ie.  $2^{(k-1)}$ ) in the Convolutional encoder. Each register is used for storing each survivor path.

The algorithm could be still improved in a field where the probability of error could be pre-estimated. In such a case a threshold could be fixed and if a path metric exceeds the threshold, it could be eliminated, thereby conserving space and computation time.

## 5. Results

### 5.1. Simulation

The main objective of this paper is to implement the IS-95 A transceiver inside a single FPGA. VHDL coding for all the modules were done and simulated. The Simulation results for Power control scheme, Convolutional encoder, CRC generators, Walsh Code generator, Data burst randomizer, Block interleaver and Viterbi decoder are shown in Figures 5-11.

The comparison results between the conventional Interleaver and the proposed Interleaver is tabulated in Table 1. In the table, the first distance is the number of bit positions by which the consecutive input bits are separated (at the output). The second distance is the number of bit positions by which the alternate input bits are separated and so on. From Table 1 it is clear that the proposed Interleaver is superior than regular Rectangular window. A simulation graph, comparing various N mod M Interleavers with respect to Distance is also included in Figure 12.

The Memory requirement of the Conventional Viterbi Decoder and the Proposed scheme are compared for various values of constraint length with convolutional encoder rate  $1/2$  and  $1/3$  is illustrated in Figure 13. For Conventional Viterbi decoders, when we change the code rate from  $1/2$  to  $1/3$ , the memory requirement (Bits Required) increases rapidly with the increase in value of Constraint length. But for the proposed decoder even for the change in code rate from  $1/2$  to  $1/3$ , the memory requirement value increases slightly. So the Proposed interleaver is adaptable for different rates of convolutional encoding.

### 5.2. FPGA Implementation

The target device chosen for implementation is XILINX Virtex V100CS144 FPGA. The IS-95A CDMA Transceiver at the Base station and at the Mobile station

are implemented in V100CS144 chip of VIRTEX FPGA family [15]. The Simulation Results of the proposed Viterbi Decoder and the proposed Interleaver are given in Figure 14 and the chip layouts of the transceivers are portrayed in Figures 15 and 16. The implementation results for the transceiver architectures at the Base station and at the mobile units are provided in Table 2. The FPGA hardware uses 88% of a 1200 slice VIRTEX FPGA device and delivers a satisfactory performance with a reduction in memory by 7.6% (for encoder rate  $1/2$ ), 40.9% (for encoder rate  $1/3$ ) and with maximum net delays much within the allowable limits of maximum data rate of 9.6Kbps.

Also the comparison results for the proposed interleaver with conventional interleaver in terms of SNR Vs BER is given in Figure 17. From the graph, for the SNR of -30 db the conventional interleaver will have 0.15 BER and the proposed interleaver will have only 0.087 Bit error rate (lesser than conventional interleaver). Thus the proposed Interleaver improves the performance of the transceivers at lower SNR levels. Also the architecture applies a new-fangled scheme for implementing Viterbi decoder and thereby results in reduced computation operations and memory requirements.

## 6. Conclusion

In this paper, a more efficient and FPGA implementation of the transceiver structures for IS-95A CDMA for forward link and reverse link written in VHDL has been presented. An optimum FPGA implementation of the same has been accomplished successfully. From the BER vs  $E/N_0$  analysis it is studied that the Interleaver proposed in this paper is more efficient than the conventional Block Interleaver. The simulation results substantiated the successful implementation of the various modules discussed earlier and the implementation in FPGA ensure that the chip will work after fabrication. FPGA implementation results in terms of decoding speed, resource usage and BER have been obtained using a tailored test bench. The paper will be extended to 4G Technology in the near future and the design could be worked on reducing power consumption

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14. Xilinx - Virtex FPGA Data Sheet





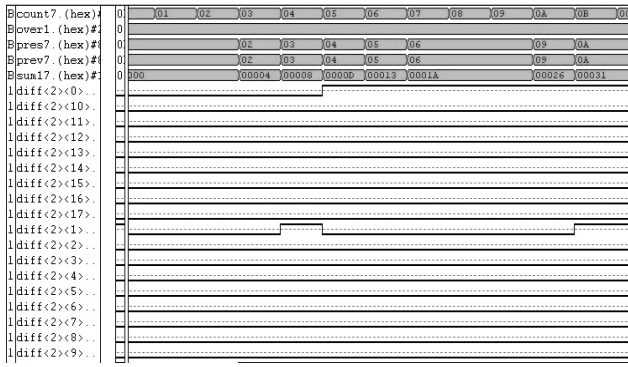


Figure5: Simulation for Power Control Scheme

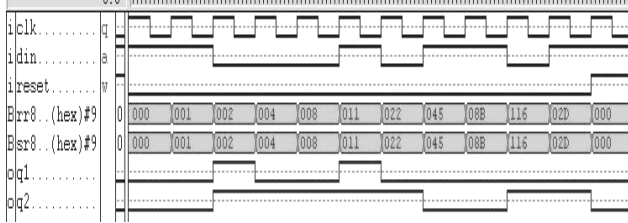


Figure 6: Simulation for convolutional encoder

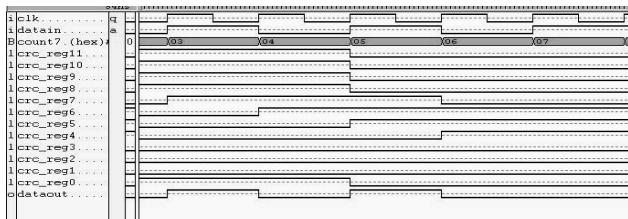


Figure7: Simulation of CRC generator

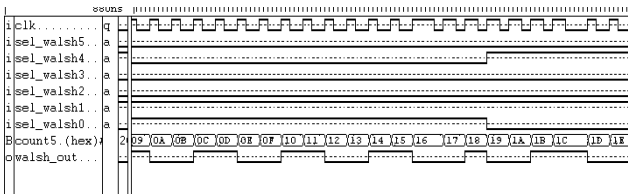


Figure 8: Simulation results of Walsh code Generator

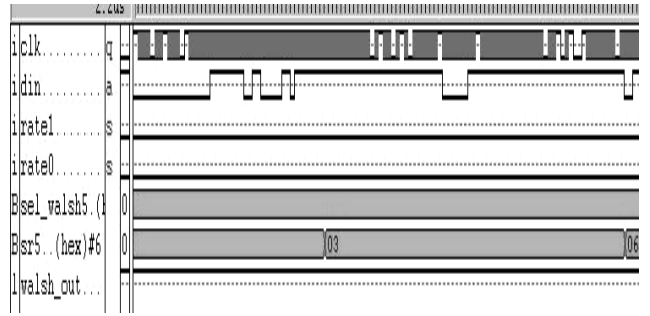


Figure9: Simulation Results of Data Burst Randomizer

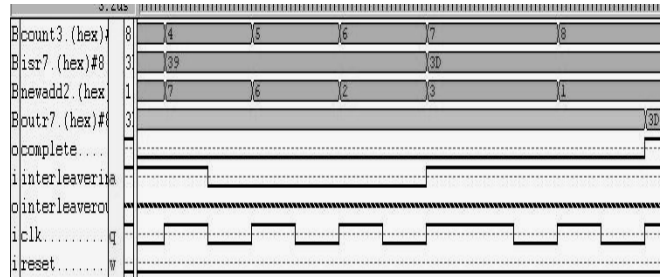


Figure 10: Simulation Results of Interleaver

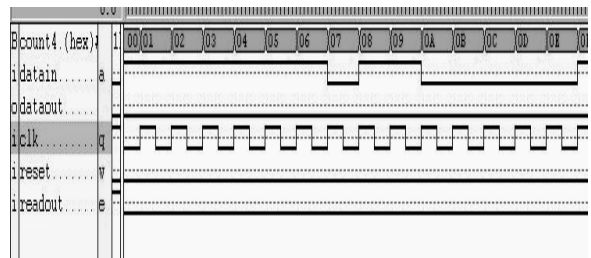


Figure 11: Simulation Results of Viterbi Decoder

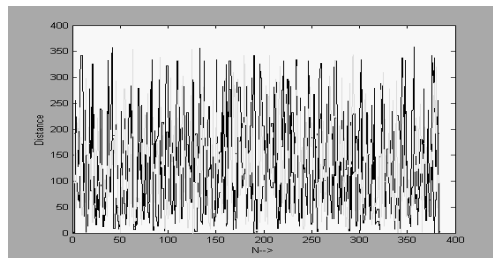


Figure 12: Comparison of the N mod M Interleavers

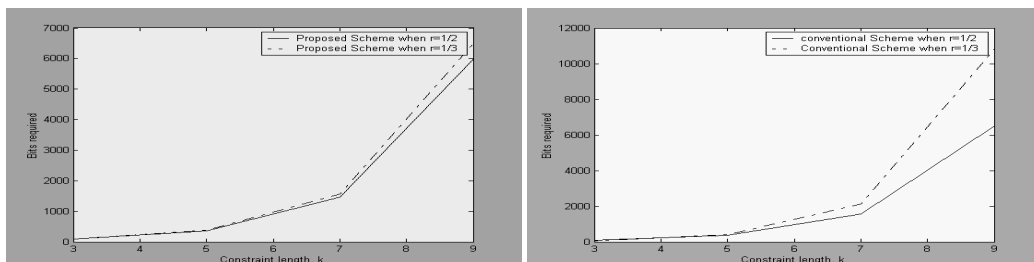


Figure 13: Comparison of the Memory requirement of the Proposed Viterbi Decoder with the conventional Viterbi Decoders



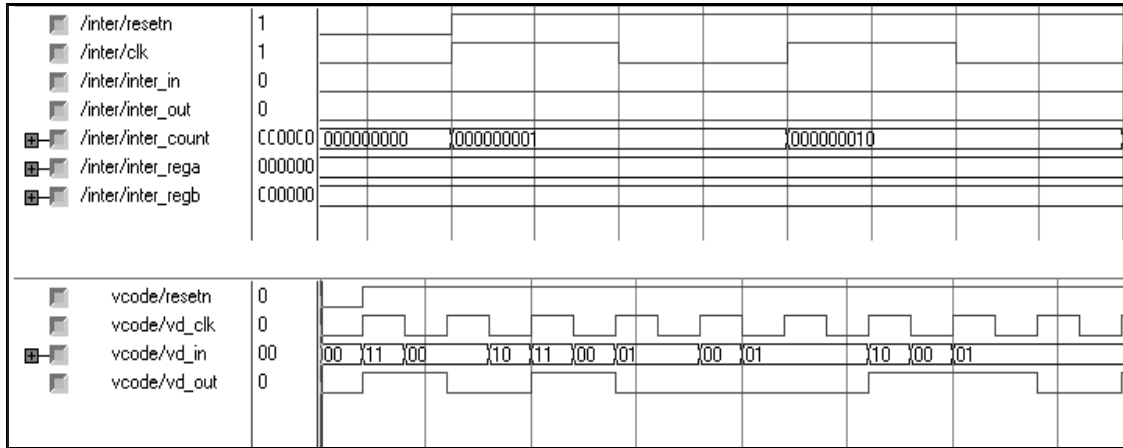


Figure 14: Simulation Results of the Proposed Interleaver and the Proposed Viterbi Decoder

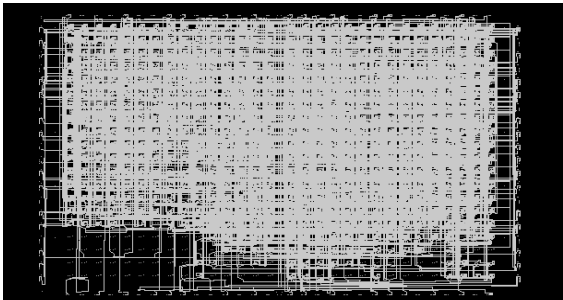


Figure 15: FPGA Layout of transceiver At the Base Station

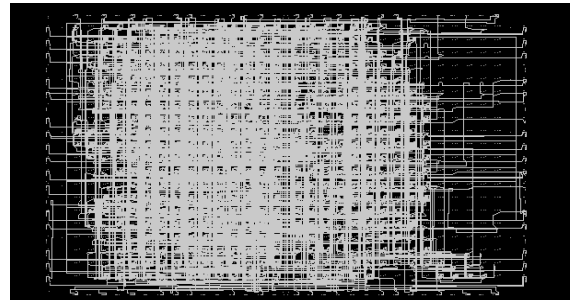


Figure 16: FPGA Layout of transceiver at the Mobile Unit

Measuring Parameter	Proposed Interleaver	Block Rectangular Interleaver
First Distance	106	23
Second Distance	170	47
Third Distance	63	71

Table 1: Comparison Results of Proposed Interleaver

Implemented Architecture	Maximum net delay	Number of Slices
Transceiver at the Mobile Unit	$10.6 \times 10^{-6}$ s	1012
Transceiver at the Base station	$11.2 \times 10^{-6}$ s	1108

Table 2: Chip Details



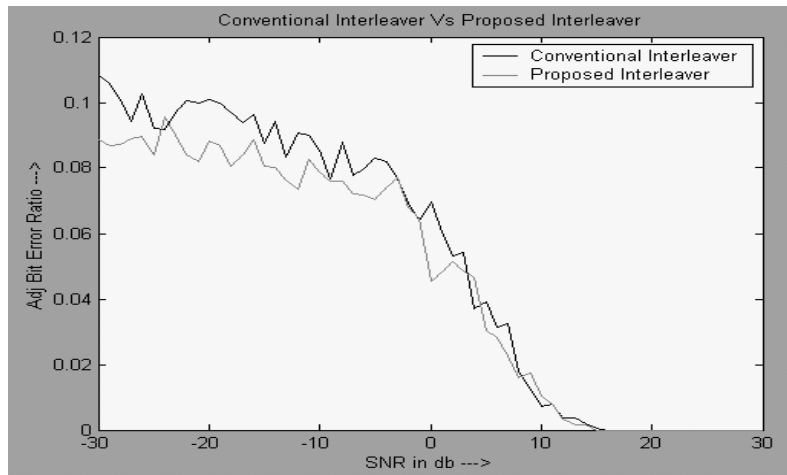


Figure 17: Comparison of Conventional and Proposed Interleavers



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